

Comparative Study on Effectiveness of On-Chip, On-Package and PCB Decoupling for Core Noise Reduction by Using Broadband Power Delivery Network Models

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Abstract

This paper discusses the effectiveness of on-chip, on-package and printed circuit board decoupling capacitors (DECAPS) used in the power delivery network (PDN) of high performance microprocessor systems for reducing the core power and ground noise over a wide frequency range. A novel method of system level broadband PDN modeling by using the impedance characterization is described. Simulation results are presented to support the validity of the PDN modeling with special emphasis on the optimization of the system level PDN impedance over a wide frequency range.

1. Introduction

The design of a noise-free power delivery network (PDN) to supply large amount of power at low voltages to microprocessor systems operating at very fast slew rate with large dynamic load and high clock frequency is a challenging task. A printed circuit board with multiple power/ground planes is commonly used in the PDN for high performance microprocessors based communication system. In general, a PDN consists of microprocessors with on-die capacitance and grid resistance, microprocessor packages, multi-layer printed circuit board (PCB), with or without DECAPS on it and voltage regulator modules (VRM). High-speed digital devices operating at low power supply voltages and high clock frequency with fast switching currents induce mid and high frequency noise into the system due to the power ground input impedance, especially due to inductance associated with the PDN loop through the package and the board. For a poorly designed PDN, the power ground noise voltages generated due to microprocessor IC circuits switching will exceed the maximum allowed noise voltage margins. As a result, the maximum operating frequency of the high-speed system reduced. Meanwhile, as the signal transmission paths share the same PDN environment, the noise will also be coupled into signals transmitted inside the PCB and package. Therefore, it is imperative to accurately model and efficiently simulate the complete PDN for designing the resonance free PDN with flat or close to flat power ground input impedance over a sufficiently wide frequency range. Since DECAPS are commonly used on PCBs and packages to eliminate the impedance resonant peaks and to lower power and ground input impedance, efficiently selecting the optimum number and types of DECAPS is a critical issue in the noise free PDN design with reduced manufacturing cost and fast design cycle. Also, in order to realize the optimum resonant free impedance over a wide frequency range using optimum number and type of DECAPS on the PCB and packages, it is equally important to perform comparative study of effectiveness of on-chip, on-package and on-PCB DECAPS by using a broadband model

of the PDN. In general a broadband model of the PDN system is the circuit or electromagnetic field based model, which exceeds the frequency range of fixed value single-lumped model. A broadband PDN model can be obtained as a ladder network with frequency independent components synthesized by fitting the S/Z/Y data of the complete PDN or PDN components such as PCB and package using a rational function approximation.[1][2].

This paper presents an efficient frequency domain simulation and analysis methodology for comparative study of the effectiveness of DECAPS in optimizing the impedance of the PDN consisting of packages and on-die circuits of microprocessors on a multi-layer PCB. First, by using an available frequency domain full wave electromagnetic field solver, for example [3], network representations of the PCB and the packages are generated. The frequency domain network characterization through the full wave electromagnetic field solver takes into account the electromagnetic field propagation and interaction properties, such as the coupling, between different components inside the PCB and the package structures. An efficient and novel methodology developed for assembling these network models of PCB, packages and die for evaluating the power ground input impedance at different microprocessor locations on the board is described in this paper. The combined PDN model is also used to evaluate the effectiveness of different DECAPS placements on the PCB, the package and the die. Different VRM models, package models, or the on-die interconnect models can also be substituted easily in the composed power delivery model for fast and accurate "what-if" analysis. In order to realize the optimum parameters of the DECAPS, based on the methodology presented in [4], a broadband equivalent circuit model for PDN components, such as PCB and package is synthesized by using the input impedance data [5][6]. Finally, the paper presents correlation between the input impedance obtained based on the analytical methodology described in the paper and from the simulation of cascaded SPICE compatible broadband behavioral model of the PCB and packages realized by using the network parameter data from the commercially available field based simulator.

Section 2 focuses on modeling a generalized PDN in terms of multi-port network; section 3 mainly describes the methodologies for computation of the power ground input impedance of the different components of the PDN and also for the complete PDN. Section 4 presents simulation and analysis results for input impedance at microprocessor core location and comparative study of different DECAP mounted on the PCB, package and on die for core power ground noise

reduction. Time domain simulation results are also presented to provide further visual information about the performance of the PDN.

2. Power Delivery Network Modeling

A generalized PDN commonly used in a high-speed digital systems consists of a multi-layer PCB mounted with VRMs, IC-packages including on-die interconnects and a number of DECAPS mounted on the top and/or bottom of the board and packages. The multi-layer PCB and packages are the critical part of the PDN for delivering the noise free power to the IC-devices. Figure 1 illustrates the block diagram of such a generalized PDN model.

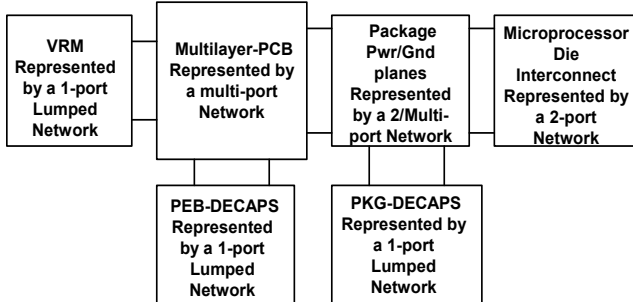


Fig. 1. Generalized PDN model

Using a commercially available electromagnetic field solver, a multi-port network representation for the PCB and packages with pre-defined locations of the DECAPS can be generated in terms of the frequency domain Z parameters. In order to study the core noise in the mid and high frequency range, the VRM used in the PDN can be represented by an open-loop, small-signal lumped circuit model. A closed-loop, small signal model of the VRM with voltage/current feedback sense point and an appropriate compensator model is required to study the core noise issues in the low frequency range. For the purpose of comparative study of effectiveness of the on-PCB, on-package and on-chip DECAPS in reducing the core noise, the VRM is considered as an ideal voltage source in this paper. The DECAPS are modeled traditionally as a one-port series RLC network with specifications provided by vendors. In order to represent the complete PDN of the high-performance digital systems, a network cascading methodology has been used for merging the multi-port-network models of PCB and packages with pre-defined locations of DECAPS. Based on the Z-matrix representation, the input impedance computation at the IC locations of the multi-port PDN is discussed to efficiently perform the "what-if" analysis for the effectiveness of on-PCB, on-package and on-chip DECAPS.

3. Input Impedance Analysis Methodology

The input impedance computation by using Z-matrix approach of a multi-port PDN is shown in Figure 2. The printed circuit board is modeled as a multi-port network. Some of the ports on the PCB are connected with the multi-port network representation of the packages, and a VRM model. The remaining ports are connected with the DECAPS models.

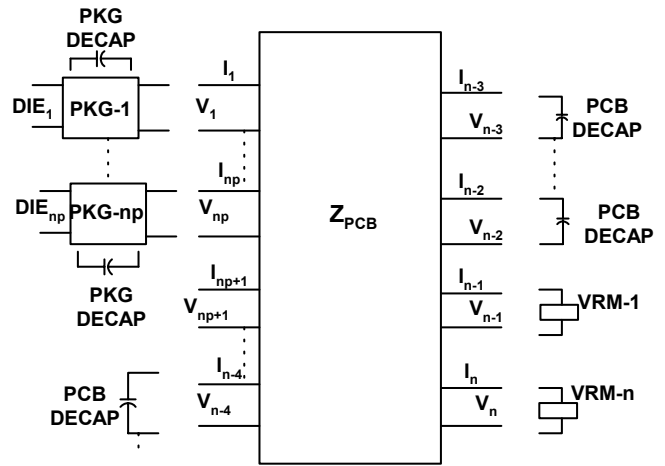


Figure 2. Z-matrix connection approach

The impedance matrices of the different components of the PDN shown in Figure 2 can be merged by matrix manipulation. Then, the power and ground input impedance at the package or die can be obtained from the resultant Z matrix of the combined PDN of the system. This hybrid modeling and analysis methodology takes into account the interaction of the electromagnetic field between different components of the PDN, without increasing the overall complexity. A flow diagram for the modeling, simulation and analysis methodology for this comparative study of the effectiveness of different types of DECAPS in the PDN is shown in Fig.3.

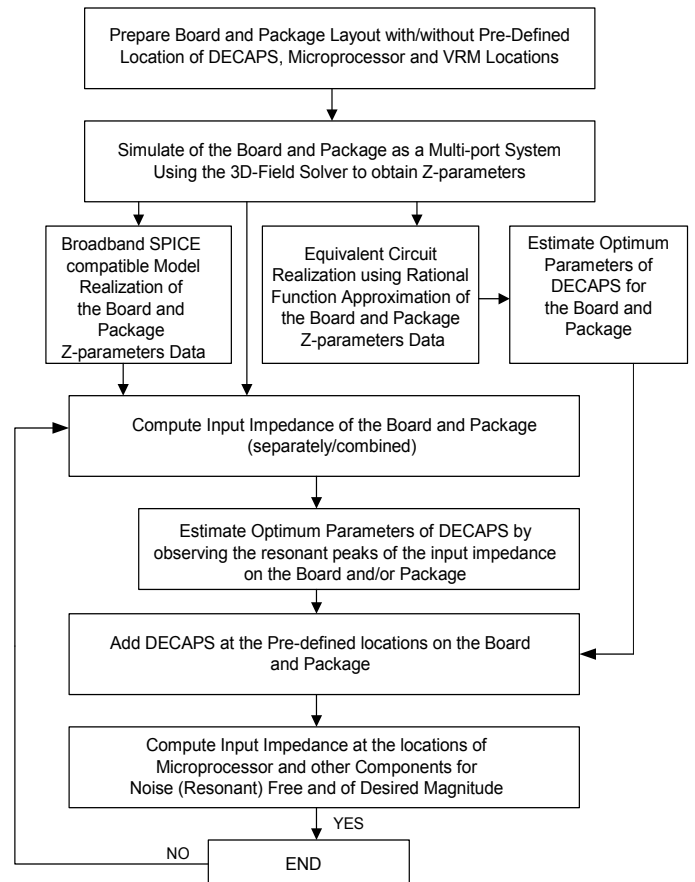


Fig. 3 PDN modeling, simulation and analysis methodology

Also, by using this hybrid modeling, simulation and analysis approach shown in Fig. 3, following “what-if” analysis can be efficiently performed:

(i) Self power and ground input impedance of the PCB (with and without DECAPS) looking into the microprocessor locations, with and without microprocessor package, as well as with and without on-die interconnections.

(ii) Transfer power/ground impedance of the PCB (with and without DECAPS) between any two microprocessor locations, from the microprocessor package, or from the die side.

The impedance characterization of the PDN components and computation of input impedance at the microprocessor core for different configurations of the PCB mounted with packages, on-die interconnections DECAPS and VRM is described next.

3.1 Impedance Characterization Method for Multiport Systems

Using Z-matrix approach, the voltage and current relations for an N-port system, in general, can be described as:

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1N} \\ Z_{21} & Z_{22} & \cdots & Z_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{N1} & Z_{N2} & \cdots & Z_{NN} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} \quad (1)$$

Note that the Z-matrix in (1) can be generated from an electromagnetic field solver. An N-port system represented by (1), for example the PCB of Fig. 2, can be terminated by

- (i) M (M < N) number of one-port terminations, such as DECAPS or VRMs, or
- (ii) K number of ports of an M-port systems, such as an M-port package with pre-defined locations of DECAPS, and ICs.

For an N-port system terminated by M number of impedance, Z_k ($k=1 \dots M$), (1) can be expressed as

$$\begin{bmatrix} [\tilde{V}_1]_{N-M} \\ [\tilde{V}_2]_M \end{bmatrix} = \begin{bmatrix} [\tilde{Z}_{11}]_{(N-M) \times (N-M)} & [\tilde{Z}_{12}]_{(N-M) \times M} \\ [\tilde{Z}_{21}]_{M \times (N-M)} & [\tilde{Z}_{22}]_{M \times M} \end{bmatrix} \begin{bmatrix} [\tilde{I}_1]_{N-M} \\ [\tilde{I}_2]_M \end{bmatrix} \quad (2)$$

Notice that in equation (2), the impedance matrix is grouped as a 2 x 2 matrix equation corresponding to group of M ports of the N-port system terminated by Z_k ($k=1 \dots M$) and the group of remaining N-M ports not terminated. The termination conditions for the M-ports can be defined as

$$[\tilde{V}_2]_M = -[\text{diag}(Z_k)]_{M \times M} [\tilde{I}_2]_M \quad (3)$$

Using (3) in (2), the new (N-M) x (N-M) impedance matrix corresponding to (N-M) ports, which are not terminated, can be obtained as

$$[\tilde{Z}_{\text{new}}] = [\tilde{Z}_{11}] - [\tilde{Z}_{12}]([\text{diag}(Z_k)] + [\tilde{Z}_{22}])^{-1} [\tilde{Z}_{21}] \quad (4)$$

Next, considering K number of ports of an M-port system A, such as a package with pre-defined locations of DECAPS and die, is connected to K number of ports of an N-port system B, such as a PCB with pre-defined locations of DECAPS, packages and VRMs. Using the 2 x 2 block matrix

representation, similar to (2), the impedance matrix for multiport systems A and B, respectively can be expressed as

$$\begin{bmatrix} [\tilde{V}_{1A}]_{N-K} \\ [\tilde{V}_{2A}]_K \end{bmatrix} = \begin{bmatrix} [\tilde{Z}_{11A}]_{(N-K) \times (N-K)} & [\tilde{Z}_{12A}]_{(N-K) \times K} \\ [\tilde{Z}_{21A}]_{K \times (N-K)} & [\tilde{Z}_{22A}]_{K \times K} \end{bmatrix} \begin{bmatrix} [\tilde{I}_{1A}]_{N-K} \\ [\tilde{I}_{2A}]_K \end{bmatrix} \quad (5)$$

and

$$\begin{bmatrix} [\tilde{V}_{1B}]_{M-K} \\ [\tilde{V}_{2B}]_K \end{bmatrix} = \begin{bmatrix} [\tilde{Z}_{11B}]_{(M-K) \times (M-K)} & [\tilde{Z}_{12B}]_{(M-K) \times K} \\ [\tilde{Z}_{21B}]_{K \times (M-K)} & [\tilde{Z}_{22B}]_{K \times K} \end{bmatrix} \begin{bmatrix} [\tilde{I}_{1B}]_{M-K} \\ [\tilde{I}_{2B}]_K \end{bmatrix} \quad (6)$$

As it is assumed that K ports of N-port system A are connected to K ports of M-port system B, the voltage and current relations for the connected ports can be expressed as

$$\begin{bmatrix} \tilde{V}_{2A} \\ \tilde{I}_{2A} \end{bmatrix}_K = \begin{bmatrix} \tilde{V}_{2B} \\ \tilde{I}_{2B} \end{bmatrix}_K = [\tilde{I}]_K \quad (7)$$

Using relation (7) in (6), the (N+M-2K) x (N+M-2K) impedance matrix for the connected system can be derived as

$$\begin{bmatrix} [\tilde{Z}_{11AB}]_{(N-K) \times (N-K)} & [\tilde{Z}_{12AB}]_{(N-K) \times (M-K)} \\ [\tilde{Z}_{21AB}]_{(M-K) \times (N-K)} & [\tilde{Z}_{22AB}]_{(M-K) \times (M-K)} \end{bmatrix} \quad (8)$$

where

$$\begin{aligned} [\tilde{Z}_{11AB}]_{(N-K) \times (N-K)} &= [\tilde{Z}_{11A}] - [\tilde{Z}_{12A}]([\tilde{Z}_{22A}] + [\tilde{Z}_{22B}])^{-1} [\tilde{Z}_{21A}] \\ [\tilde{Z}_{12AB}]_{(N-K) \times (M-K)} &= [\tilde{Z}_{12A}]([\tilde{Z}_{22A}] + [\tilde{Z}_{22B}])^{-1} [\tilde{Z}_{21B}] \\ [\tilde{Z}_{21AB}]_{(M-K) \times (N-K)} &= [\tilde{Z}_{12B}]([\tilde{Z}_{22A}] + [\tilde{Z}_{22B}])^{-1} [\tilde{Z}_{21A}] \\ [\tilde{Z}_{22AB}]_{(M-K) \times (M-K)} &= [\tilde{Z}_{11B}] - [\tilde{Z}_{12B}]([\tilde{Z}_{22A}] + [\tilde{Z}_{22B}])^{-1} [\tilde{Z}_{21B}] \end{aligned} \quad (9)$$

This methodology of connecting K ports of two N and M port systems can be extended to connect several ports between three multi-port systems. As an example, consider three multi-port systems A, B, and C of ports N, M and O respectively. Assuming K ports are connected between systems A and C and L ports connected between systems B and C, the 2 x 2 block representation of these systems can be expressed as

$$\begin{bmatrix} [\tilde{V}_{1A}]_{N-K} \\ [\tilde{V}_{2A}]_K \end{bmatrix} = \begin{bmatrix} [\tilde{Z}_{11A}]_{(N-K) \times (N-K)} & [\tilde{Z}_{12A}]_{(N-K) \times K} \\ [\tilde{Z}_{21A}]_{K \times (N-K)} & [\tilde{Z}_{22A}]_{K \times K} \end{bmatrix} \begin{bmatrix} [\tilde{I}_{1A}]_{N-K} \\ [\tilde{I}_{2A}]_K \end{bmatrix}$$

$$\begin{bmatrix} [\tilde{V}_{1B}]_{M-L} \\ [\tilde{V}_{2B}]_L \end{bmatrix} = \begin{bmatrix} [\tilde{Z}_{11B}]_{(M-L) \times (M-L)} & [\tilde{Z}_{12B}]_{(M-L) \times L} \\ [\tilde{Z}_{21B}]_{L \times (M-L)} & [\tilde{Z}_{22B}]_{L \times L} \end{bmatrix} \begin{bmatrix} [\tilde{I}_{1B}]_{M-L} \\ [\tilde{I}_{2B}]_L \end{bmatrix}, \text{ and}$$

$$\begin{bmatrix} [\tilde{V}_{1C}]_{O-K-L} \\ [\tilde{V}_{2C}]_{K+L} \end{bmatrix} = \begin{bmatrix} [\tilde{Z}_{11C}]_{(O-K-L) \times (O-K-L)} & [\tilde{Z}_{12C}]_{(O-K-L) \times (K+L)} \\ [\tilde{Z}_{21C}]_{(K+L) \times (O-K-L)} & [\tilde{Z}_{22C}]_{(K+L) \times (K+L)} \end{bmatrix} \begin{bmatrix} [\tilde{I}_{1C}]_{O-K-L} \\ [\tilde{I}_{2C}]_{K+L} \end{bmatrix} \quad (10)$$

The expressions for system A and B in (10) can be combined as

$$\begin{bmatrix} \left[\begin{array}{c} \tilde{V}_{1A} \\ \tilde{V}_{1B} \end{array} \right]_{N+M-K-L} \\ \left[\begin{array}{c} \tilde{V}_{2A} \\ \tilde{V}_{2B} \end{array} \right]_{K+L} \end{bmatrix} = \begin{bmatrix} \left[\begin{array}{cc} \tilde{Z}_{11A} & \\ & \tilde{Z}_{11B} \end{array} \right] & \left[\begin{array}{c} \tilde{Z}_{12A} \\ \tilde{Z}_{12B} \end{array} \right] \\ \left[\begin{array}{c} \tilde{Z}_{21A} \\ \tilde{Z}_{21B} \end{array} \right] & \left[\begin{array}{cc} \tilde{Z}_{22A} & \\ & \tilde{Z}_{22B} \end{array} \right] \end{bmatrix} \begin{bmatrix} \left[\begin{array}{c} \tilde{I}_{1A} \\ \tilde{I}_{1B} \end{array} \right]_{N+M-K-L} \\ \left[\begin{array}{c} \tilde{I}_{2A} \\ \tilde{I}_{2B} \end{array} \right]_{K+L} \end{bmatrix} \quad (11)$$

Note that equation for system C in (10) for connecting three multiport systems is similar to (6) for connecting two multiport systems. Also, (11) for systems A and B together, in the 2 x 2 block matrix representation, is similar to (5). As described earlier in case of connecting K ports of two systems of N-ports and M-ports respectively, the impedance matrix similar to (8) for the resultant (N + M + O - 2K - 2L) ordered system as a result of connecting systems A and B to system C can be derived using following conditions:

$$\begin{bmatrix} \left[\begin{array}{c} \tilde{V}_{2A} \\ \tilde{V}_{2B} \end{array} \right]_K \\ \left[\begin{array}{c} \tilde{V}_{2C} \\ \tilde{V}_{2D} \end{array} \right]_{K+L} \end{bmatrix}_{K+L} = \left[\tilde{V}_{2C} \right]_{K+L} \quad (12)$$

$$\begin{bmatrix} \left[\begin{array}{c} \tilde{I}_{2A} \\ \tilde{I}_{2B} \end{array} \right]_K \\ \left[\begin{array}{c} \tilde{I}_{2C} \\ \tilde{I}_{2D} \end{array} \right]_{K+L} \end{bmatrix}_{K+L} = -\left[\tilde{I}_{2C} \right]_{K+L} = \left[\tilde{I} \right]_{K+L}$$

3.2 Application to PDN of Microprocessor Systems

The impedance characterization method for multiport system described in the previous section can be applied to the PDN of microprocessor system consisting of die, packages with pre-defined locations for DECAPS and PCB with pre-defined locations for VRMs, packages and DECAPS. As an example the method has been applied to a PCB with pre-defined location for VRM, DECAPS and a package with pre-defined locations of die and DECAPS. The model for the die on a package can be described using a 2 x 2 matrix, such as

$$\begin{bmatrix} Z_{11}^{die} & Z_{12}^{die} \\ Z_{21}^{die} & Z_{22}^{die} \end{bmatrix}_{2 \times 2} \quad (13)$$

The impedance matrix for the package, assuming that the first port is at the die location, usually at the top of package, the second port is at the C5-balls location at the bottom of the package, and remaining ports are at the pre-defined nd_pkg number of locations for DECAPS, at the top or bottom of the package, can be represented by an nk x nk matrix:

$$\begin{bmatrix} Z_{11}^{pkg} & Z_{12}^{pkg} & \dots & Z_{1nk}^{pkg} \\ Z_{21}^{pkg} & Z_{22}^{pkg} & \dots & Z_{2nk}^{pkg} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{nk1}^{pkg} & Z_{nk2}^{pkg} & \dots & Z_{nknk}^{pkg} \end{bmatrix}_{nk \times nk} \quad (14)$$

Note that the order of the matrix, nk = nd_pkg + 2.

For several packages at the pre-defined n_pkg number of locations mounted on the PCB, the impedance matrix for the k-th package becomes:

$$\begin{bmatrix} Z_{11}^{pkg(k)} & Z_{12}^{pkg(k)} & \dots & Z_{1nk}^{pkg(k)} \\ Z_{21}^{pkg(k)} & Z_{22}^{pkg(k)} & \dots & Z_{2nk}^{pkg(k)} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{nk1}^{pkg(k)} & Z_{nk2}^{pkg(k)} & \dots & Z_{nknk}^{pkg(k)} \end{bmatrix}_{nk(k) \times nk(k)} \quad (15)$$

where, k = 1...n_pkg. Note that, as the number DECAPS on each package is different, the order of the impedance matrix (15) for each of the packages may not be same.

Next, the overall impedance matrix for a PCB with pre-defined n_pkg number of locations for packages, nd_pcb number of locations for DECAPS on PCB and the pre-defined location for a VRM can be represented by an np x np matrix:

$$\begin{bmatrix} Z_{11}^{PCB} & Z_{12}^{PCB} & \dots & Z_{1np}^{PCB} \\ Z_{21}^{PCB} & Z_{22}^{PCB} & \dots & Z_{2np}^{PCB} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{np1}^{PCB} & Z_{np2}^{PCB} & \dots & Z_{nnp}^{PCB} \end{bmatrix}_{np \times np} \quad (16)$$

where, np = n_pkg + nd_pcb + 1.

Using the process of merging K ports of two systems described earlier, the merging or connection of die with package can be performed first using the matrices (13) and (15) followed by merging the resultant package with the PCB. Finally, the package and the PCB can be terminated at the desired pre-defined locations for DECAPS and VRMs using the process of terminating an N-port system with M number of one port terminations described earlier. The impedance matrix of DECAPS used on PCB and package is the diagonal matrix of the order equal to number of DECAPS with diagonal entries as the impedance of a DECAP, which is the series combination of R_d, the equivalent series resistance (ESR), L_d, the equivalent series inductance (ESL) and C_d, the capacitance.

One can see that the Z-matrix approach to model the different components of the PDN described in this paper provides a broadband mathematical model of the PDN of a microprocessor system. This broadband mathematical model of the complete PDN system is used efficiently to perform frequency domain comparative study of effectiveness of on-PCB, on-package and on-chip DECAPS for core noise reduction and the performance optimization of the overall PDN impedance of a microprocessor system over a wide frequency range.

3.3 Broadband SPICE Compatible PDN Model

It is important to note that a SPICE compatible broadband behavioral model of the PCB and packages, separately or combined can be generated by using a commercially available circuit model generator/extractor, such as [BBS-Sigrity]. The Z-parameters obtained from the simulation of package or PCB structure from the field solver can be imported in the broadband SPICE tool to generate a SPICE compatible, multiport sub-circuit model of the PCB and package. These sub-circuit models with input output ports and ports to connect the DECAP model can be cascaded easily as shown in Fig. 4 for the frequency domain and time domain simulation of the complete PDN by using a SPICE simulator.

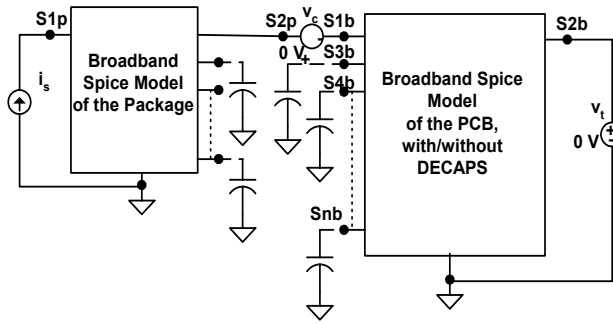


Fig. 4 Broadband SPICE models of PDN components

Although, such PDN models are very useful in analyzing the design options for the resonant free PDN, the non-transparent topology and complexity of the generated model makes it impractical to apply certain techniques such as described in [4] to estimate the optimum size and types of DECAPS to be added at the PCB and packages. In order to alleviate this problem, it is needed to efficiently synthesize a broadband equivalent circuit model from the frequency-dependent response of the PDN components obtained in this paper from the commercially available field solver.

3.4 Broadband Equivalent Circuit Model of PDN

A systematic methodology for the synthesis of a SPICE compatible broadband equivalent circuit models from the frequency-dependent data is presented in [1]. Based on the vector fitting procedure described in [5], the rational transfer function approximation of the input impedance parameter data obtained from the simulation of PCB or package using commercially available electromagnetic field solver is used in this paper. Next, by applying the procedure of synthesizing the real and complex pole pair of a transfer function as discussed in [6], a broadband equivalent circuit of PCB or package is obtained as shown in Fig. 5.

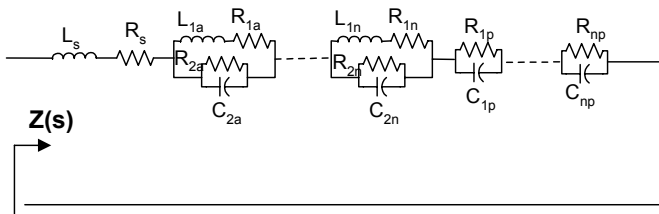


Fig. 5 Broadband equivalent circuit model of PCB or package

Using the synthesized broadband equivalent model of the PCB and package as shown in Fig. 5, a broadband equivalent PDN model of a microprocessor system with circuit model of DECAPS at different stages is shown in Fig. 6.

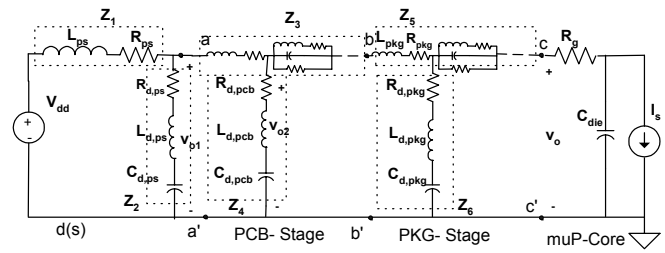


Fig. 6 Broadband equivalent PDN model

The broadband equivalent PDN model of Fig. 6 is suitable for the procedure described in [4] to estimate the optimum ESR, ESL and capacitance of the DECAPS to realize the resonant free, close to flat input impedance of the PDN. Note that, unlike the broadband PDN model described in sections 3.1 and 3.3 respectively, the disadvantage of the equivalent model synthesized from the rational function approximation of the frequency dependent response is that the information about locations of DECAPS on the PCB and package disappears. However, using the optimum DECAPS estimated from Fig. 6 and the process described in section 3 for estimating the input impedance, the effectiveness of on-PCB, and on-package DECAPS, along with on-chip capacitance on reducing the core noise in the PDN of a microprocessor system can be investigated efficiently. Also, the model can be used for efficient time domain and frequency domain simulation.

4. Simulation and Analysis Results

For the purpose of demonstrating the PDN modeling, simulation and analysis methodology described in section 3, a typical 8-layer system board mounted with a BGA package and a VRM on the top layer, and pre-defined locations for DECAPS on the top and bottom layers is considered as an example in this paper. Different configurations of the system board have been used to evaluate the input impedance characteristics at the locations of the microprocessor core. These configurations are different in the number, and the type of DECAPS placed on the PCB and package, around the microprocessor, in order to realize the overall power and ground input impedance close to a specified target impedance over a wide frequency range. Also, different configurations are considered to perform the comparative study on the effectiveness of on-chip, on-package and on-PCB DECAPS for core noise reduction.

First the multi-port impedance matrices for the board and package without DECAPS at the predefined locations are obtained from the frequency domain simulation of the system board and the package separately by using a full wave electromagnetic field solver.

Next, at the microprocessor core location, the input impedance characteristic for different configurations of the PCB, the package and the package merged or cascaded with the PCB is obtained by the following procedures:

- (i) using the analytical methodology described in section 3.1
- (ii) using the vector fitting method

- (iii) using the SPICE simulation of the broadband models of the PCB and package, and

using the SPICE simulation of the broadband equivalent circuit of the PCB and the package synthesized from their respective input impedance characteristics obtained by (i) or (ii)

Finally, for the purpose of the comparative analysis, the DECAPS are selected and placed at the pre-defined locations on the top and bottom layer of the PCB and also on the top layer of the package as close as possible to the microprocessor core. It is important to note that for the process (i) and (iii) the full wave electromagnetic field solver is used only for the simulation of the PCB and the package with pre-defined locations of DECAPS and to obtain the corresponding Z-matrix data. Once the Z-matrix data from the field solver is obtained, it can be used for further comparative study of the different types of DECAPS on the PCB, package and die using process (i) or (iii). Therefore, simulation using the field solver need not be repeated to obtain the input impedance at the microprocessor core location with different number and values of DECAPS on the top and/or bottom layer of the board and package.

At the microprocessor location, the self-input impedance of the PCB with pre-defined locations of DECAPS, obtained using process (i)-(iv) are shown in Figure 6.

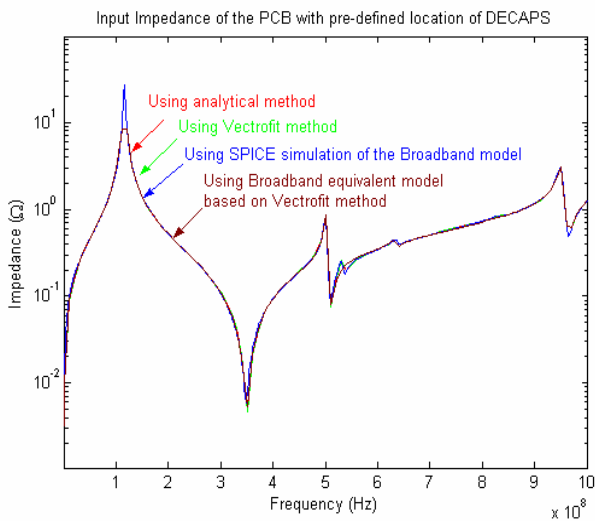


Fig. 6 Input impedance of the PCB without any DECAPS at pre-defined locations and VRM shorted.

Note that the plots shown in Fig. 6 for the input impedance at the location of the microprocessor obtained using the process (i)-(iv) matches very well. This validates the analytical methodology developed and described in this paper for estimating the input impedance.

The self input impedance for the package with 20 pre-defined locations for DECAPS is obtained using process (i)-(iv). The graphic plots for of these self-input impedances are shown in Fig. 7, which shows that the input impedance obtained using process(i)-(iv) are well matched.

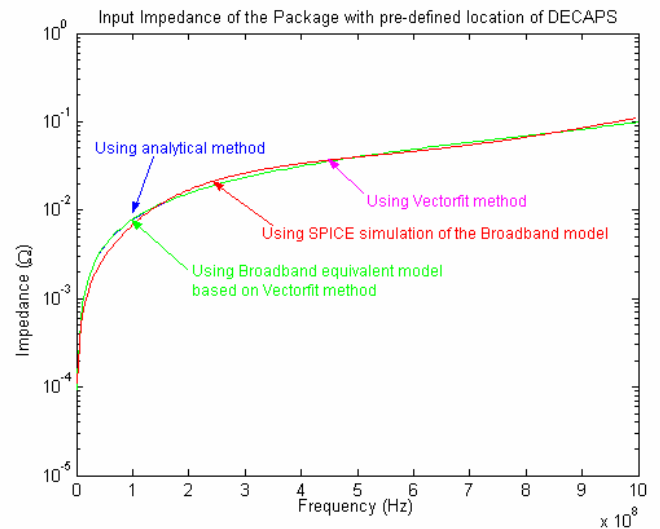


Fig 7. Input impedance of the package without any decaps mounted at 20 pre-defined locations.

Using the analytical method described in section 3.1, the overall self input impedance at the microprocessor location for the package without any DECAPS at the 20 pre-defined locations merged with the PCB without any DECAPS. Figure 8 shows good correlation between the overall self-input impedance obtained using the process (i)-(iii).

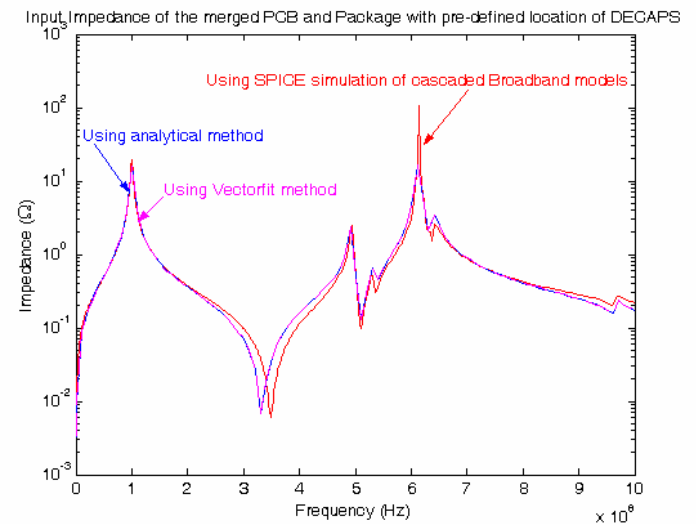


Fig. 8 Input impedance of the PCB without any DECAPS at pre-defined locations plus package without any DECAPS at pre-defined location and VRM shorted

The input impedance plots of the PCB without DECAPS and with optimized DECAPS obtained from the broadband equivalent circuit of Fig. 2 are shown in Fig. 9. These plots in Fig. 9 are obtained based on the analytical method by distributing the DECAPS at 31 location and also by using the DECAPS as a lumped model in the broadband equivalent circuit model of Fig. 5.

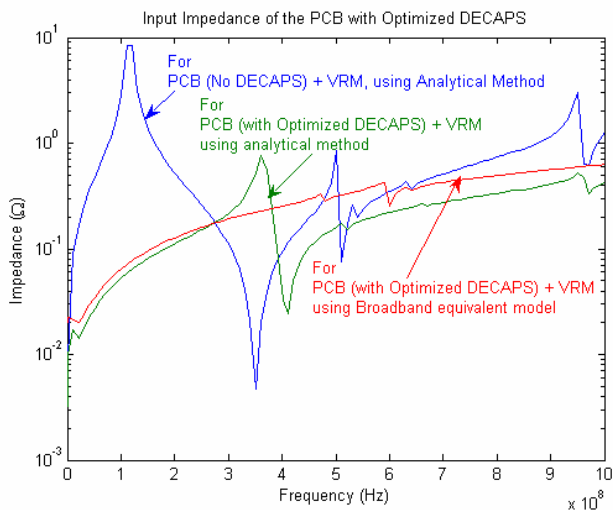


Fig. 9 Input impedance of the PCB without and with optimized DECAPS at pre-defined locations and VRM shorted

Next, the effectiveness of DECAPS added on the PCB, the package and the die capacitance on the input impedance at the microprocessor location is investigated for the following configurations:

- (i) Considering die capacitance of 20 nF with no DECAPS added at the pre-defined locations on the PCB and the package
- (ii) Considering die capacitance of 20 nF with 31 DECAPS of value $C = 4.82$ nF, $ESL = 297.2$ pH, $ESR = 0.787 \Omega$ added at the pre-defined locations on the PCB and no DECAPS on the package
- (iii) Considering die capacitance of 20 nF with 20 DECAPS of value $C = 270$ pF, $ESL = 300$ pH, $ESR = 1.49 \Omega$ added at the pre-defined locations on the package and no DECAPS on the PCB
- (iv) Considering die capacitance of 20 nF with 31 DECAPS of value $C = 4.82$ nF, $ESL = 297.2$ pH, $ESR = 0.787 \Omega$ added at the pre-defined locations on the PCB and with 20 DECAPS of value $C = 270$ pF, $ESL = 300$ pH, $ESR = 1.49 \Omega$ added at the pre-defined locations on the package.
- (v) Considering die capacitance of 20 nF with 31 DECAPS added at the pre-defined locations on PCB and package with optimum value obtained using the broadband equivalent circuit of Fig. 5 as $C = 40.654$ nF, $ESL = 282.58$ pH and $ESR = 0.2765 \Omega$.

The impedance magnitude plots for these configurations, (i) – (v) are shown in Fig. 10. In Fig. 10, it can be noticed that the resonant peaks above 200 MHz has been eliminated by the die capacitance with no DECAPS at the pre-defined locations on the package and the PCB. The addition of DECAPS on the package reduces the resonant peaks in around 50 MHz. The DECAPS mounted at the pre-defined

locations on the PCB, in addition to the DECAPS on the package further reduces the resonant peaks at 50 MHz.

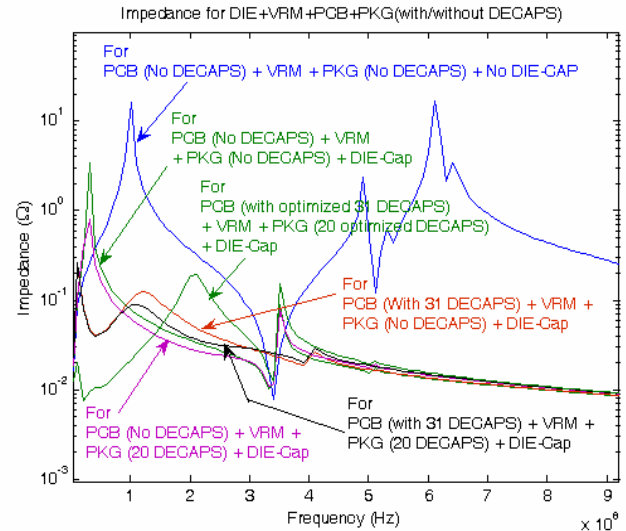


Fig. 10 Input impedance of the PCB without/with any DECAPS at pre-defined locations plus package without/with any DECAPS at pre-defined location and VRM shorted

5. Discussions and Conclusions

Based on a network representation of different components used in a PDN, an efficient simulation and analysis methodology for optimizing the PDN performance of a system board mounted with microprocessor packages, VRM and DECAPS has been presented in this paper. The method provides a capability of fast, accurate modeling of the physical structure and efficient computational algorithm for performance optimization of DECAPS required for a PDN. An efficient analytical matrix computation schemes is described for the input impedance computation of the PCB merged with packages and terminated by DECAPS and VRM models at the pre-defined locations on the PCB. Simulation results that are efficiently obtained by using the analysis method described in this paper are presented for different DECAP configurations of the PCB and package for comparative study of the effectiveness of on-die capacitance, on-package DECAPS and on-PCB DECAPS. These simulation results are further correlated with those obtained from the cascaded broadband model as well as the broadband equivalent circuit model realized using the vector fitting method. The utility of this broadband equivalent circuit model in computing the optimum parameters of the DECAPS to be placed on the PCB and package to realize the resonant free and close to flat impedance magnitude is also demonstrated.

6. Reference

- [1] Pinello, W., Morsey, J., and Cangellaris, A. C., "Synthesis of SPICE-Compatible Broadband Electrical Models for Pins and Vias", *Proc. 51th Electronic Components and Technology Conf.*, Orlando, FL, May 2001
- [2] Choi, W., Min, S., Kim, J., Swaminathan, M., Beyene, W., and Yuan, X., "Modeling and Analysis of Power

- Distribution Networks for Gigabit Applications", *IEEE Trans. Mobile Computing.*, pp. 299-312, vol. 2, no. 4, October 2003
- [3] PowerSI by Sigrity, Inc.
 - [4] Mandhana, O., "Modeling, Analysis and Design of Resonant Free Power Distribution Network for Modern Microprocessor Systems", *IEEE Trans. Advanced Packaging*, pp. 107-120, vol. 27, no. 1, February 2004
 - [5] Gustavsen, B., and Semlyen, A., "Rational Approximation of Frequency Domain Responses by Vector Fitting", *IEEE Trans. Power Delivery*, pp. 1052-1061, vol. 14, no. 3, July 1999
 - [6] Antonini, G., "SPICE Equivalent Circuits of Frequency-Domain Responses", *IEEE Trans. Electromagnetic Compatibility*, pp. 502-512, vol. 45, no. 3, August 2003
 - [7] L. Smith, et al., "Power distribution system design methodology and capacitor selection for modern CMOS technology", *IEEE Trans. Advanced Packag.*, pp. 284-290, vol. 22, August 1999.
 - [8] SPEED2000 by Sigrity, Inc.