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Power Delivery Network Optimization for Laptop and Desktop Computer Platforms

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Abstract

A method is presented for optimizing power delivery networks (PDN) for computer platforms. Frequency domain simulation is applied as a basis for the optimization and augmented by time domain validation to assure voltage noise targets are met at the CPU, memory controller and I/O controller. A custom “voltage test tool” controls PDN current activity and an oscilloscope measures PDN noise voltage. Analyses and measurements are presented for both laptop and desktop platforms. Performance is maintained, or even improved, for cost-sensitive designs with cost savings of 10% to 45%. Capacitor count reductions of 20% are achieved for area-constrained designs.

Index Terms

Power Integrity (PI), Decoupling Capacitor (Decap), Low Cost, Power Optimization

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Introduction

In today's high-speed systems even small power delivery network (PDN) noise margin violations may cause system failure. IC power consumption increases with higher performance and greater functionality. Despite a per-device power consumption decrease, total IC power consumption continues to increase with the latest IC fabrication technology, even with the corresponding decrease in voltage levels. This implies a dramatic increase in PDN current, as seen in Figure 1. However, reduced power delivery network (PDN) voltage is accompanied by reduced PDN noise margin for both DC IR drop and AC noise. Significant challenges exist for PDN designers due to this simultaneous decrease of noise margins and increase of noise generation (current).

On one side, designers must provide higher performance PDNs to meet tight noise margins - often with increased design complexity and higher cost. On the other hand, managers have pressure to achieve lower cost targets to assure products are competitive. In this paper we are concerned with design techniques to achieve AC noise margin through application of decoupling capacitors (decaps). We discuss a method of PDN optimization and validation for laptop and desktop platforms to achieve desired trade-off between PDN performance and total decoupling capacitor cost.

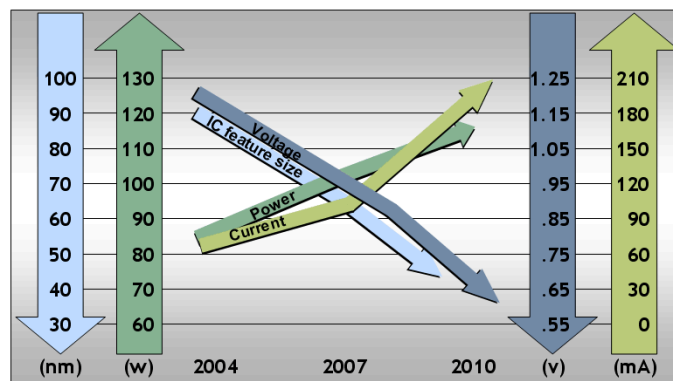


Figure 1 Decreasing voltage and increasing power imply dramatically increasing current (data sourced from ITRS 2008 tables)

Though time domain noise is very intuitive for engineers, and is ultimately the criterion by which PDN performance is judged, design optimization based on transient simulation has proven much more compute resource intensive relative to frequency domain simulation. Designers typically apply frequency-domain characterization for passive, linear-time-invariant components and circuits, followed by time-domain circuit simulation for a system of concatenated components and measurement validation. This design approach allows a system-level time domain stimulus to be changed with only a new circuit simulation – all the component models are reused. It is usually easier to identify, troubleshoot and suppress PDN noise issues with frequency domain simulation for two reasons: (1) global PDN resonances occur that must be identified and suppressed; (2) decoupling capacitors behave as series RLC resonators, whose decap values may be selected based on desired resonance frequency and loop inductance of the decap seen by the PDN.

For frequency domain analysis input impedance is often applied to represent PDN design performance. A two-port network is applied for an explanation of what was considered in this paper. In Figure 2, the self impedances Z_{11} and Z_{22} are also called the input impedances. Each input impedance is the ratio of its input voltage to its input current when the other port is open. Port currents are considered as the stimulus for PDN analysis. Since port noise voltage is linearly proportional to both current and input impedance, lower input impedance corresponds to higher PDN performance. Z_{12} and Z_{21} are called transfer impedance and represent coupling between the two ports. The transfer impedance and is applied for isolation analysis. For the general case, both port currents exist and the total port voltage will have contributions from both input impedance and transfer impedance. In this paper the input impedance alone was applied to determine PDN performance. The transfer impedance degrades PDN performance mostly near global resonances. Since the designs examined were known not have global resonances the choice was successful and results are unaffected if transfer impedance is included.

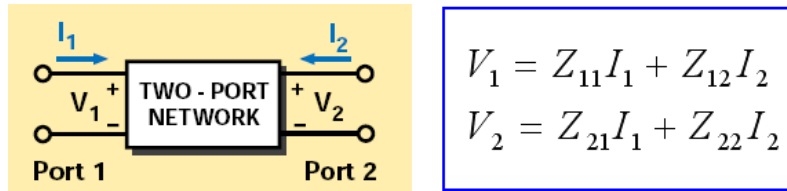


Figure 2 Input impedance definition in two-port network

For PDN frequency domain analysis a target impedance is applied as the design specification. Target impedance is defined as the ratio of voltage tolerance and current fluctuation, refer to Figure 3. The target impedance is not generally a constant and most often only its amplitude is specified. Designers can estimate the target impedance by applying data in IC datasheet or requested from IC vendors directly. The frequency domain PDN design and optimization object is to assure input impedance magnitude below target impedance within the frequency range of interest.

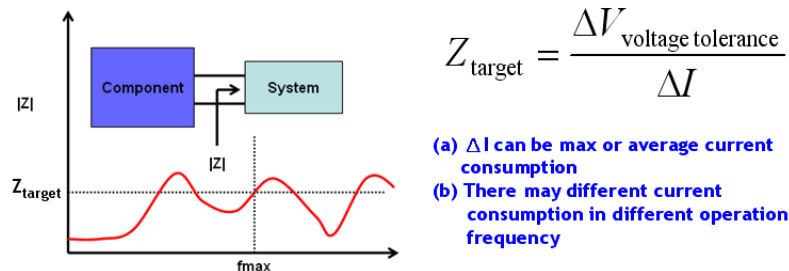


Figure 3 Target impedance definition in real system

To reduce input impedance (frequency domain) and stabilize power supply voltage noise (time domain), decaps are used extensively on boards and in packages and even in the silicon ICs. Decaps play a vital role in AC power delivery to local components. Some people perceive decaps as “charge wells” and recommend exclusive application of large-valued decaps. This is an incomplete and DC-centric view that leads to an improper recommendation. Relative to a given component, decaps certainly provide charge for switching currents but the capacitance forms a low impedance series RLC resonator with the loop inductance from the component to the decap. The loop inductance is the sum of

the effective series inductance (ESL) of the decap, mounting inductance of each the component and the decap and the PDN spreading inductance between the component and the decap. Large-valued, so-called “bulk” capacitors are placed local to the voltage regulator module (VRM). Bulk caps provides low frequency (typically below 1MHz) switching current throughout the PDN. Board mounted decaps provide mid frequency (typically below 100MHz) switching currents to components in close proximity. In-package decaps are typically more expensive to implement but typically double or triple the switching current frequency range relative to board mounted decaps. This is due to a reduced loop inductance and application of lower-valued decaps. On-chip decaps provide switching currents at higher frequencies, again because of reduced loop inductance and smaller valued decaps.

The frequency response of a PDN input impedance will behave generally as shown in Figure 4. There are many impedance peaks at different frequency ranges and these peaks will create large power noise to system. Decaps of various value and location are added to suppress these impedance peaks by providing localized, frequency-selective low impedance paths between PDN planes.

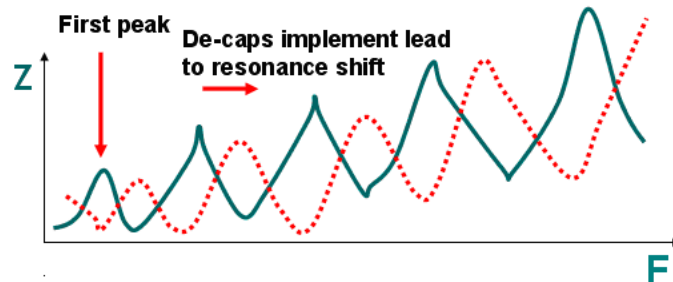


Figure 4 PDN frequency response and the effect of decaps

One of the most difficult challenges for board design is to determine how many decaps are needed, of what value and where to mount them. Most board designers are conservative and apply significantly more decaps than are required to assure low noise power delivery. Many of those decaps may prove to be unnecessary in the end. However, this practice is common for two reasons: (1) it is often better to incur the cost of extra decaps and the associated design area rather than fail to meet PDN noise margins and deal with a re-spin, (2) it is much easier to add decaps at the post-placement/pre-route stage than to push signal nets around late in the design to add more decaps.

This paper applies a commercially available EDA tool (OptimizePI™ from Sigrity) to automatically select decap values and find optimum decap locations for laptop and desktop platforms to assure CPU, MCH and ICH meet PDN impedance constraints and validate AC noise margins are met. The tool’s underlying frequency domain analysis is high capacity; able to address entire platform boards and packages. All PDN parasitics are considered in the broadband analysis: {R,L,C}, coupling, planes, traces, voids, pads, vias, wirebonds, dispersive materials, etc. There are four objectives available for the PDN optimizations: best performance vs. cost, best performance vs. area, best performance vs. number of decaps, best overall performance. Available decaps for placement are selected from a library, which includes both component and mounting cost for each decap. A

frequency-dependent target impedance may be defined or a default, design-dependent threshold value is selected automatically. After initial frequency domain PDN analysis a type of global genetic optimization is performed to determine optimal decap selection and placement. The optimization is controlled by the average impedance ratio (AIR), a scalar measure of impedance averaged over all components at all frequencies. Optimal design schemes are provided over a range of total decap cost. At each cost component PDN input impedances, a decap placement table and bill of materials (BOM) are provided for the optimum design. Per-component transient current sources may be defined and total noise determined for the optimum schemes. Loop inductance display and a quick what-if analysis support fine tuning of optimized schemes, which can help to improve the design or simplify the BOM. After optimization the selected decap design schemes were implemented and lab measurements were performed to determine the PDN noise level for comparison to the simulated results.

Measurements applied a TDS7104 oscilloscope with 1GHz bandwidth. The setup shown in Figure 5 was implemented for PDN noise measurement for CPU for Desktop platform. A custom hardware Voltage Test Tool (VTT) is applied. The VTT is controlled by a PC with a USB cable. The VTT is implemented to draw a high current with uniform distribution across the CPU. For other power components the stress-test software 3DMark2001 was executed to generate PDN voltage noise.

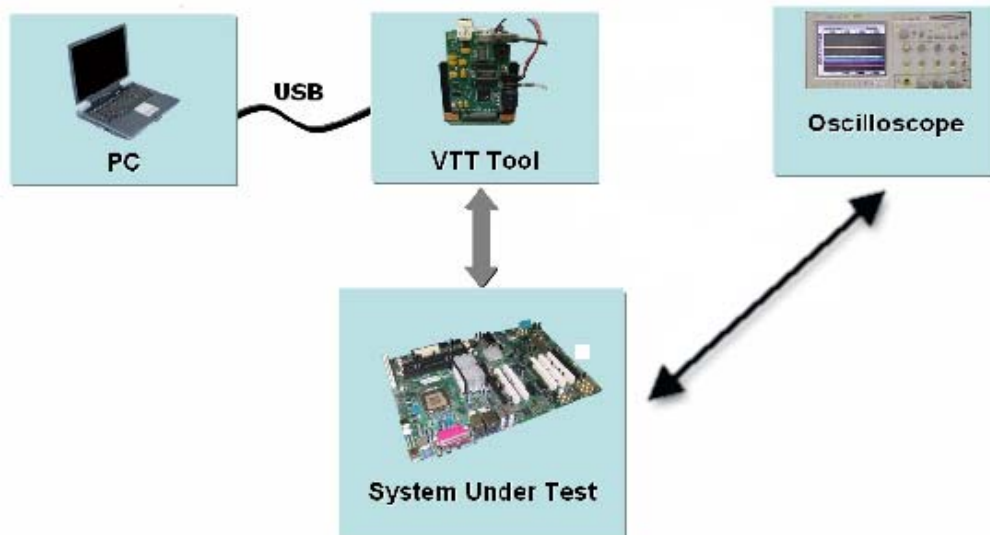


Figure 5 PDN noise measurement setup for CPU

Laptop Platform Optimization

For a laptop platform motherboard the desire is to achieve the same PDN performance as the original design but with minimum cost. A 6-layer board is considered. The two PWR/GND rails of interest are nets VCC_CORE/GND and V1.05S/GND. The VRM on the board is modeled as a 5.9m Ohm resistor and mounted on the TOP layer. A total of 21 decaps are available in a library for application in this design, each with RLC format electrical. To allow public disclosure generic models and cost information was applied.

The electrical models are from www.murata.com and the decap cost values are from www.digikey.com. The frequency range of optimization is from 10KHz to 500MHz. The optimization selected a default threshold impedance target based on the original design. The design objective of maximum performance vs. cost was selected.

For optimization of CPU decaps, the VCC_CORE and GND nets are on the Top and Bottom layers, respectively. The local shapes of these nets are very narrow. The CPU input impedance observation is U86, as highlighted in Figure 6.



Figure 6 Input impedance observation for VCC_CORE/GND rail

After this first optimization is finished system-level and component-level information is displayed graphically to support intuitive tradeoff of performance and cost, as shown in Figure 7. The optimized scheme 119 with the same performance at lower cost is chosen as follows:

In the top XY plot of Performance vs. Minimum Cost the system-level PDN performance measure of Average Impedance Ratio (AIR) is displayed. The AIR of the original design is shown with a red asterisk in the bottom right portion of the plot. The AIR of the original design is 21.0. The AIR of all optimized designs are shown as blue marks. The optimized scheme with AIR value closest to 21.0 is selected - scheme 119. The selected optimal scheme is indicated with a red circle around its blue mark in the top XY plot and is highlighted in the table on the left.

In the bottom XY plot the input impedances at the CPU for the original and optimized designs are shown to be nearly identical; the red and blue traces, respectively. The original decap cost is \$1.96 and the cost of the optimized scheme is only \$1.74, which is 11% cost reduction for very similar PDN impedance performance.

This component-level verification is important to assure the optimization did not average-out an impedance peak for one of the components under consideration. It is also important to explore lower cost design schemes because performance often degrades slowly as cost is lowered and additional cost savings may well be available.

Other simulation results include: a placement table and BOM for each optimal design scheme that contains decap placement and selection information; a summary report that containing all the optimization information for all optimal schemes.

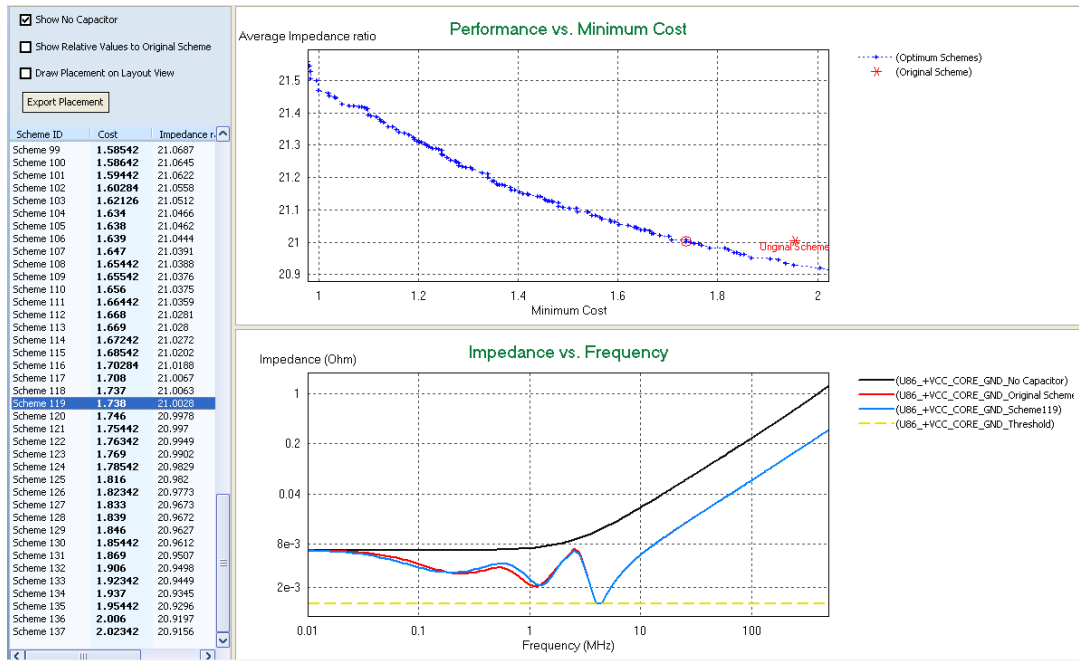


Figure 7 Optimization results for VCC_CORE/GND rail

Figure 8 shows the measured PDN noise before and after optimization on power rail VCC_CORE: 9.8mV and 13mV, respectively. The impedance in the 500kHz to 1MHz range is higher and likely what causes the increase in measured PDN noise level for the optimized designing. Both noise values are within the AC noise margin of 20mV for this component so the 11% cost reduction may not be the maximum cost savings available for this design.

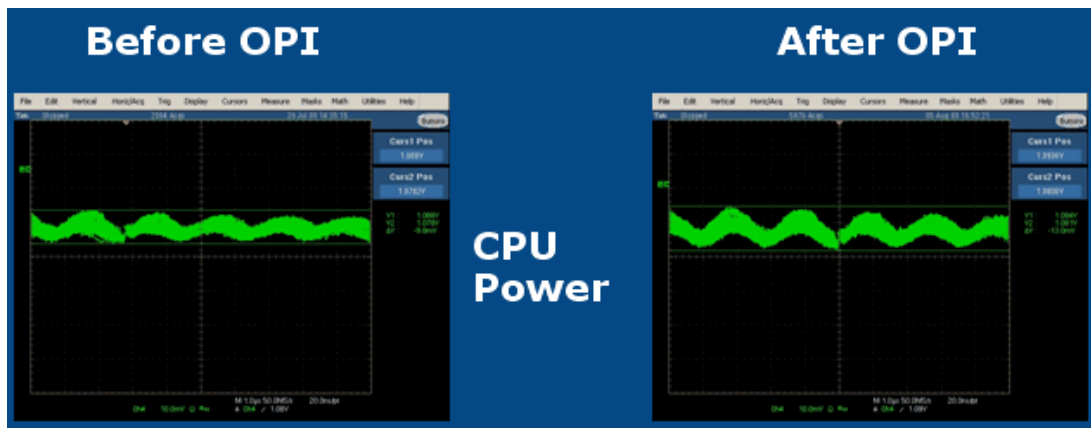


Figure 8 Measured VCC_CORE PDN noise at CPU U86 before and after optimization

For optimization of decaps on the V1.05S power rail the nets VCC5 and GND are on the Top and Bottom layers, respectively. The input impedance locations for optimization are highlighted in Figure 9: U69 (MCH), ICH U74 (ICH) and CPU U86 (CPU).

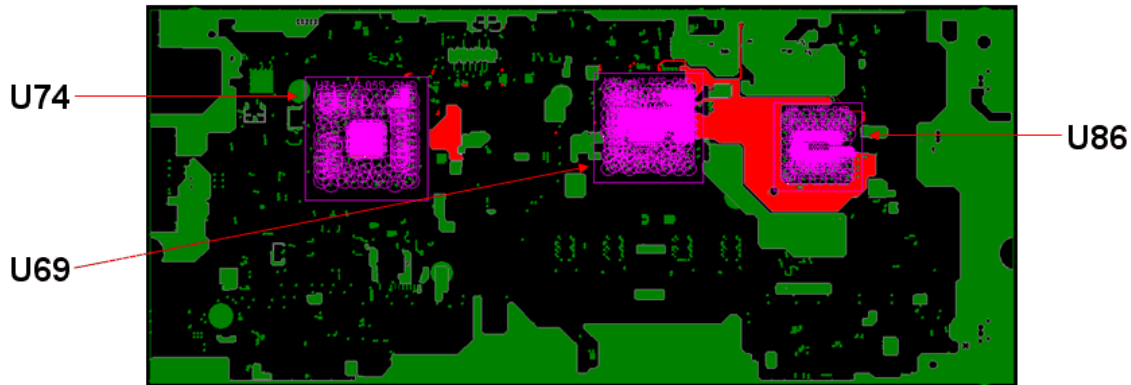


Figure 9 Input impedance observations for V1.05S/GND rail

After this second optimization is finished system-level and component-level information is displayed graphically, as shown in Figure 10. The optimized scheme 14 with the same performance at lower cost is chosen in the same manner as the optimal scheme was selected for the first CPU PDN optimization. The PDN performance is expected to be similar to the original design but at significantly lower cost. Again, the component-level input impedance is observed, for U69 in this case, to assure similar a AIR value implies similar component-level input impedance. The original design cost is \$3.48 and the optimized design cost is \$1.82, for substantial 48% cost saving of \$1.66.

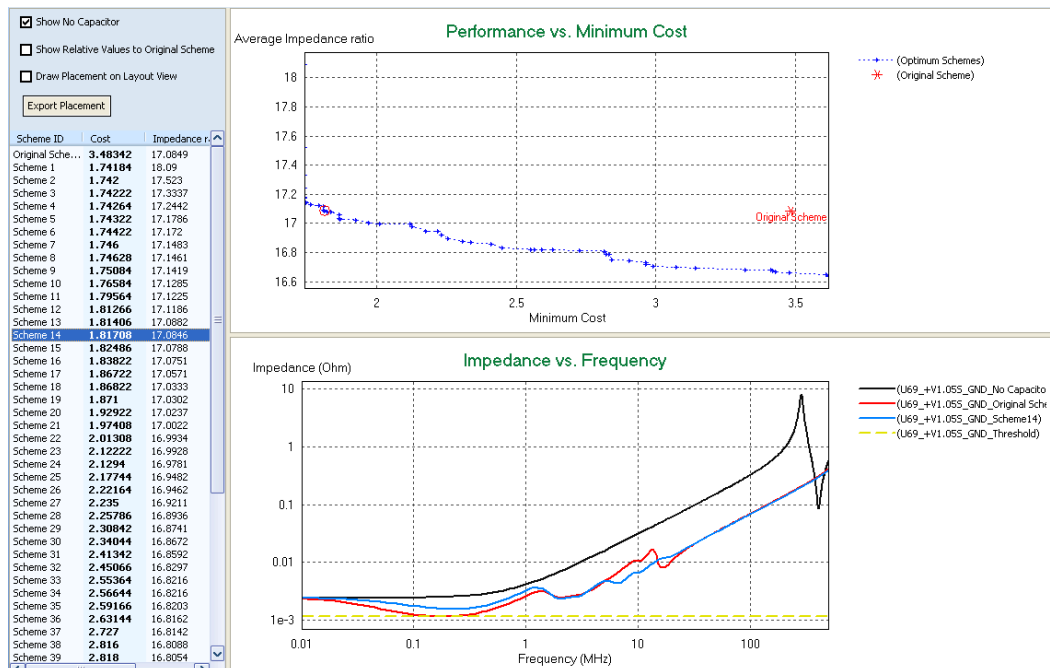


Figure 10 Optimization results for V1.05S/GND rail

Figure 8 shows the measured VCC_CORE PDN noise before and after optimization: 9.8mV and 13mV, respectively. The impedance in the 500kHz to 1MHz range is higher

and likely what causes the increase in measured PDN noise level for the optimized design. Both noise values are within the AC noise margin of 20mV for this component so the 11% cost reduction may not be the maximum cost savings available for this design. Figure 11 shows the measured PDN noise before and after optimization at U69 (MCH) on system power rail V1.05S: 35.4mV and 29.2mV, respectively. Although the optimized design impedance is higher than the original design impedance below 1MHz, it is significantly less in the 5-15MHz range. Therefore, the PDN AC noise is reduced in this case relative to the original design. Both the original and the optimized design are within the AC noise margin of 50 mV for this power rail. The PDN AC noise for ICH and CPU components behave similarly and are still within allowable noise margins for both original and optimized designs. As before, 48% cost reduction again may not be the maximum cost savings available for this design.

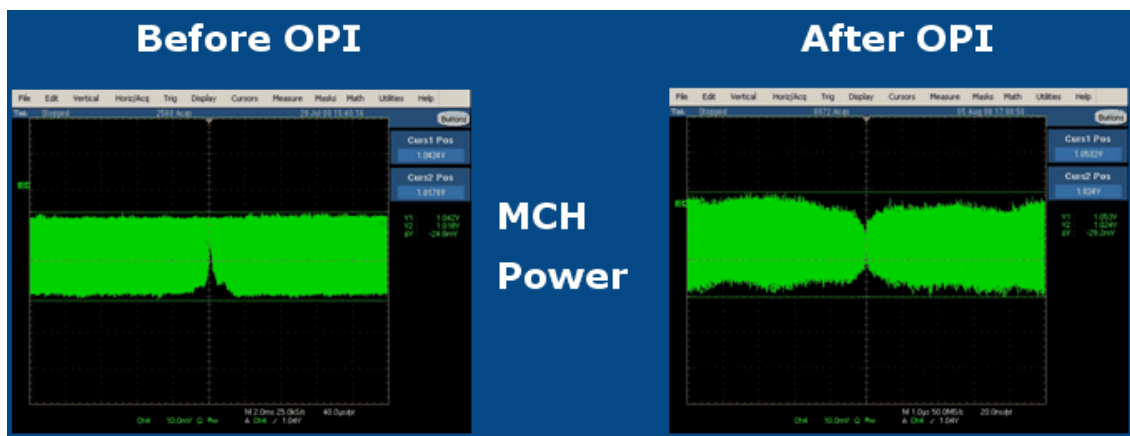


Figure 11 Measured V1.05S noises at MCH U69 before/after optimization

Desktop Platform Optimization

For a desktop platform motherboard the desire is to delete as many decaps on the board as possible with the least impact on PDN performance. A 4-layer board is considered. The single PWR/GND rail is comprised of nets VCCP and GND on the Top and Bottom layers, respectively. The VRM on the board is modeled as a 5m Ohm resistor and mounted on the TOP layer. A similar but smaller decap library with non-proprietary models and cost information was applied as for the laptop platform. The frequency range of optimization is again 10KHz to 500MHz. For this application, the design objective of maximum performance vs. number of decaps was selected. The CPU input impedance observation is JIPR, as highlighted in Figure 12.

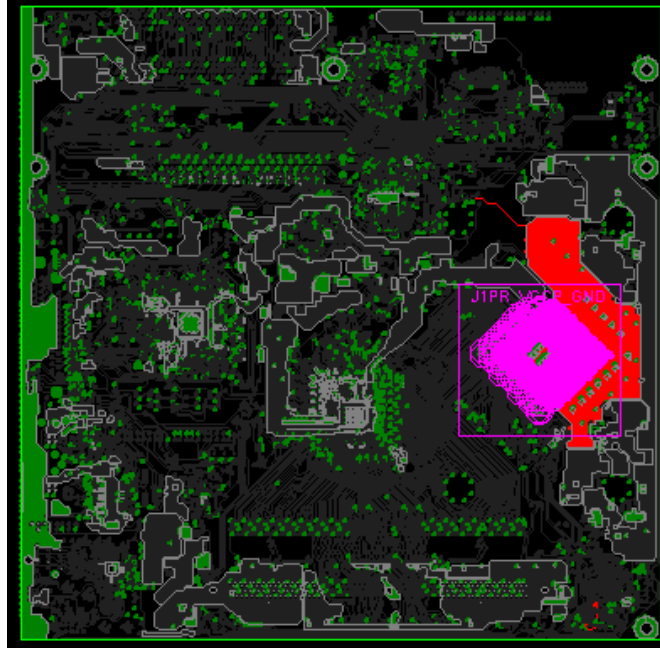


Figure 12 Input impedance observation for VCCP/GND rail

After this third optimization is finished the same familiar system-level and component-level information is displayed. The results clearly indicate 3 of the original 15 decaps may be eliminated to yield the same system-level AIR impedance performance measure. The decaps (C21TH, C63VR and C72VR) may be deleted as summarized in the decap placement table of Figure 13.

* Refdes	Decap Placement Part No.	ID
C21TH	---	---
C63VR	---	---
C64VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C65VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C66VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C67VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C68VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C69VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C70VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C72VR	---	---
C73VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C75VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C76VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C78VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3
C80VR	CAP_1206-22UF_20%_6_3V_1206_22UF	3

Figure 13 Decap Placement table generated by OptimizePI for VCCP/GND

Figure 14 shows the measured VCCP PDN noise before and after optimization at J1PR (CPU): 9.8mV and 9.6mV, respectively. Both noise levels are within the 10mV AC noise margin. The optimization showed we can eliminate 20% of the decaps with a slightly improved PDN noise level.

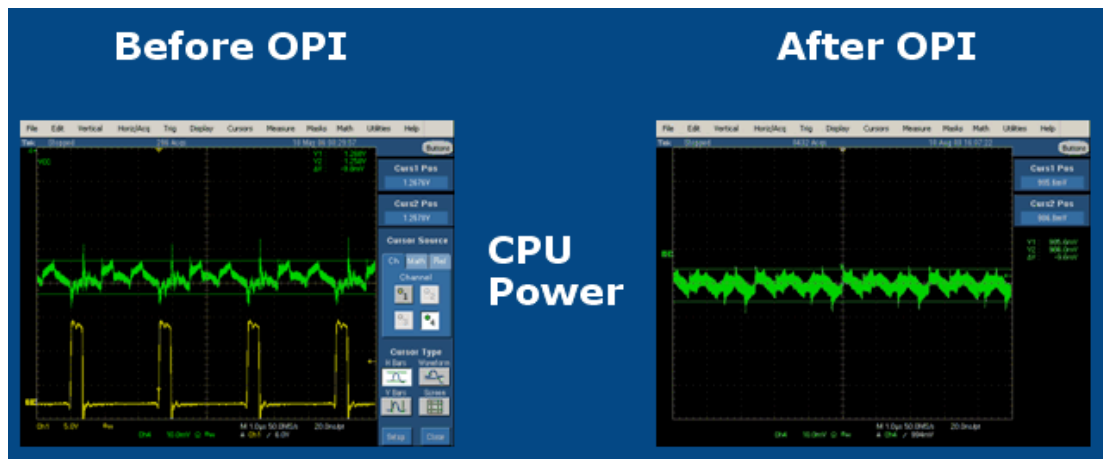


Figure 14 Measured VCCP noises at CPU J1PR before/after optimization

Conclusion

This paper reviews several important concepts for frequency domain PDN characterization and demonstrates a successful application of simulation-based frequency domain PDN optimization. The optimization method can yield similar PDN performance with reduced cost or reduced decap count. The decap designs were done very carefully and yet in some cases significant cost savings could still be realized. By selecting a different performance vs. cost tradeoff higher performance could be obtained for the same cost or decap count. Measurements were performed to verify that similar time domain noise levels are expected for original and optimized designs if similar frequency domain input impedance levels are predicted.

As component vendors move toward frequency domain input impedance specifications for system boards rather than very specific decap selection and placement design guidelines this type of frequency domain based optimization procedure will help to assure performance targets are met at minimum cost.

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